CONFIDENTIAL

Technical and Quality general Requirements
for Printed Circuit Boards

TQR-SEL-Rev12

This document is property of Selcom and contains confidential and proprietary information. This document or part of it cannot be copied or shared with third parties without an explicit written authorization from Selcom. Any offenders are liable to pay all relevant damages.
If a conflict occurs between the English and translated versions of this document or part of it, the English version will take precedence.
In this document, the words "shall" or "must" are used to identify a requirement.
If any discrepancy is found in the documentation, Supplier shall immediately contact Selcom to clarify the specification.
In any case Selcom reserves the right to arbitrate among own documents in order to determine the authentic interpretation of own will.

Rev	***Description***	***Author***	***Date***
11	General update	Domenichini	01st April 2012
12	**General update: revised all paragraphs, except:** 2.2; 2.4; 2.5; 2.6; 2.14; 2.15; 3.5; 3.8.3; 4.3; 4.4; 5.2; 7.1; 7.3; 8.3. **Added paragraphs:** 2.18; 3.7.2; 6.4.7; 7.6; 8.6.	Domenichini	10th July 2015

INDEX

1.INTRODUCTION....4
1.1.Glossary of main terms used in Selcom documents....4
1.2.Documents layout....8

2.GENERAL REQUIREMENTS....9
2.1.Acceptance criteria....9
2.2.Quantities....10
2.3.Supply approval....10
2.4.Documentation....11
2.5.No Transfer....11
2.6.Prices....11
2.7.Guarantee of quality....11
2.8.Oldest acceptable batch....11
2.9.Documents priority order....11
2.10.Applicable documents....12
2.11.UL marking....13
2.12.FIFO production logic....13
2.13.All-In-Home processes....14
2.14.Scraps and rework policy....14
2.15.Country of Manufacture....15
2.16.Files modifications by supplier....15
2.17.Test coupon layout....15
2.18.Netlist file....15

3.GENERAL MANUFACTURING SPECIFICATIONS....17
3.1.Base materials....17
3.2.Dimensional Requirements....18
3.3.Holes dimension and tolerance....19
3.4.Warping and twisting....19
3.5.V-cut (scoring)....20
3.6.IPC-A-600 minimum requirements....20
3.7.Silver-Through-Hole technology....22
3.7.1.Requirements of STH Construction....23
3.7.2.Copper-Paste-Through-Hole technology....24
3.8.Requirements for Carbon-conductive PCBs....25
3.8.1.Typical design of carbon contact key pad....25
3.8.2.Configuration cross-section of carbon contact....25
3.8.3.Configuration design of carbon crossover jumper....26
3.8.4.Specifications table....26
3.8.5.Homologated Carbon Inks....27
3.8.6.Homologated Over Coating material....28

4.DIMENSIONAL REQUIREMENTS OF CONDUCTORS LAYOUT....28
4.1.Minimum annular ring....28
4.2.Width of conductors and insulation....28
4.3.Conductors imperfections....28
4.4.Etching....29

5.GALVANIC COATINGS....29
5.1. Tear test....29
5.2. Copper plating inside via holes....29
5.3. Gold plated contacts....29

6.SURFACE TREATMENTS....30

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

6.1.Solderable Surface finishing....30
6.2.Wettability....30
6.3.Solder resist protective covering....31
6.4.Via holes and solder resist treatment....32
6.4.1.Free from solder mask (CASE 1)....33
6.4.2.One-side plug-in (CASE 2)....33
6.4.3.Vias corners covered with solder mask (CASE 3)....33
6.4.4.Via fill (CASE 4)....34
6.4.5.Via test-point (CASE 5)....34
6.4.6.Via hole closed and sealed by solder resist (CASE 6)....35
6.4.7.Via fill and cap (CASE 7)....36
6.5.Peelable solder mask....36
6.6.Silkscreen (Legend)....36

7.TESTS....38
7.1.Visual test....38
7.2.Electrical test....38
7.3.Mechanical test....38
7.4.Scrap pieces....38
7.5.Repairs and reworks....39
7.6.Microsection....40

8.SUPPLY METHODOLOGY....42
8.1.Identification of the circuits....42
8.2.Cleaning operations....42
8.3. Packaging....42
8.3.1 Moisture Barrier Bags....42
8.3.2 Carton boxes....44
8.3.3 Pallets....45
8.4.Documents enclosed with each supply....45
8.5.Documents enclosed with first supply....46
8.6.Documents format....46

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

1. INTRODUCTION

1.1. Glossary of main terms used in Selcom documents

- Selcom = Business Group composed by different sister Companies (Selital, Procond, Selcom Shanghai, etc.). In present document, every reference to "Selcom" is valid also with reference to other sister Companies belonging to the same Business Group. Every communication from supplier must be properly addressed to the specific Company which issued the Purchase Order.

- PCB = Bare (unpopulated) finished Printed Circuit Board, as received by Selcom from supplier. (PCBs = plural form).

- PCBA = assembled (populated) PCB, that means PCB with components soldered on. (PCBAs = plural form).

- part number = p/n = the exact and complete name of PCB, as showed in Selcom Purchase Order. (p/ns = plural form).

- TQR = the present document (see description in §1.2)

- MA documents = collection of Selcom relevant technical documentation about a specific p/n, as described in TQR §1.2.

- MA file = package of files including gerbers and MA documents, as described in TQR §1.2.

- batch = quantity of pieces belonging to the same supplier's production period, identified by the supplier through the "batch code" written on each PCB.

- batch code = lot code = date code = the unique code identifying a batch and its original production date. It must be generated through specific rules typically described in MA file.

- shipment = quantity of pieces identified by a single shipment document.

- wettability = solderability = property of a pad surface to be easily soldered by Selcom.

- solder voiding = presence of permanent cavities into solder joints after Selcom soldering process.

- supplier = company that sells PCBs to Selcom.

- sub-supplier = company that produces or processes materials for supplier.

- final customer application = application field of the electronic device into which the PCB will operate, after Selcom assembly.

- PTH = Pin-Through-Hole (plated).

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

- piece = single piece = unit piece = minimum single repetitive unit (or kit of units) included in the same delivery panel.

- delivery panel = minimum single delivery unit, made by a solid planar collection of identical pieces. The word “panel” means “delivery panel” in Selcom documents, if not otherwise specified.

- working panel = single production unit used by PCB supplier, made by a solid planar collection of various delivery panels.

- X-out = single piece marked as defective within a delivery panel.

- breakaway = when present, frame planar structure which holds and collects various single pieces to form one single solid delivery panel.

- gerber = gerber file = file with used by printed circuit board (PCB) industry software to describe shape and dimension of the PCB images, such as: copper layers, solder mask, legend, etc. (gerbers = plural form).

- STH = Silver-Through-Hole technology = a technology where the electrical connection into vias is realized by means of a conductive silver paste instead of a copper galvanic plating.

- CPTH = CTH = Copper-Paste-Through-Hole technology = a technology where the electrical connection into vias is realized by means of a conductive copper paste instead of copper galvanic plating.

- raw materials = base materials = those materials listed in TQR §2.3.

- 1 mm = 10^{-3} m.

- 1 µm = 1 um = 10^{-3} mm = 10^{-6} m.

- 1 mil = 10^{-3} inches = 0,0254 mm. (mils = plural form).

- 1 ppm = 1 part per million = 0,0001%.

- 1 kPa = 10^{3} Pascal = pressure measure unit.

- CTI = Comparative Tracking Index, measured according to IEC 60112 Fourth edition (Jan 2003).

- CTI PLC = Comparative Tracking Performance Level Category, as defined in standard UL746A dated 06th Sep 2001, table 23.1; see following:

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Tracking Index (Volts)	PLC
600 or more	0
between 400 and 599	1
between 250 and 399	2
between 175 and 249	3
between 100 and 174	4
less than 100	5

- ➔ BGA = Ball Grid Array = a surface-mounted component with spherical terminations located under the body of the component.

- ➔ HASL = HAL = Hot Air Surface Leveling = solderable surface finishing applied through immersion of PCB inside a bath of molten solder alloy, then leveled over pads by means of hot air blown over them.

- ➔ ENIG = Electroless Nichel + Immersion Gold chemical solderable surface finishing.

- ➔ ITIN = Immersion Tin chemical solderable surface finishing.

- ➔ OSP = Organic Solderability Preservative = organic surface finishing applied over bare copper to protect its solderability.

- ➔ chemical surface finishings = non-galvanic metallic solderable surface finishings different than HASL. Examples of chemical surface finishings: Immersion Tin; Immersion Silver; ENIG.

- ➔ **,** = comma in numbers is meant as decimal point.

- ➔ e.g. = “exempli gratia” (latin) = “for example” (english).

- ➔ via = via hole = electrical connection between different conductors layers in a printed circuit board, realized by means of a vertical electrically-conductive hole. (vias = plural form).

- ➔ critical quotas = quotas that, if mismatched, could lead to severe issues on PCBA or final device like for example: safety issues; reliability issues; conformity to law regulations; severe limitations to efficiency or usability; severe issues during assembling or next processes; etc. Cpk of critical quotas shall be greater than 1,33. Mismatch of one or more critical quotas may lead to 100% sorting or reject of batch.

- ➔ important quotas = non-critical quotas that, if mismatched, could lead to relevant issues on PCBA or final device, like for example: partial limitations to efficiency or usability; significant issues during assembling; need of sorting or rework; etc.

- ➔ critical defect = a defect that is likely to result in hazardous or unsafe conditions for individuals using, maintaining, or depending upon the products; or to prevent performance of the tactical

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

function of a major end item. A critical defective is a unit of product that contains one or more critical defects.

- major defect = A defect, other than critical, that is likely to result in failure, or to reduce materially the usability of the unit of product for its intended purpose. A major defective is a unit of product that contains one or more major defects.

- minor defect = A defect that is not likely to reduce materially the usability of the unit of product for its intended purpose, or is a departure from established standards having little bearing on the effective use or operation of the unit of product. A minor defective is a unit of product that contains one or more defects.

- RoHS = *"Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment"*, or latest revision / amendment.

- RoHS declaration = a formal declaration written and undersigned by PCB supplier stating that his goods shipped to Selcom are fully conforming to all requirements of RoHS. If not otherwise required by Selcom, the "RoHS declaration" does not necessarily include laboratory analysis test reports.

- RoHS - compliant PCB = PCB in compliance with RoHS = a PCB which fits RoHS requirements and which is able to withstand the higher thermal stresses given by multiple lead-free soldering processes.

- shelf life = maximum length of time for a PCB (kept sealed into proper packaging bag) after its original production date, before it becomes unfit for being used by Selcom.

- expiration date = original production date + shelf life.

- supplier identification symbol = a unique symbol assigned to PCB supplier by Selcom before first supply, and typically required to be used as first char of lot-code syntax printed on PCBs.

- CoC = Certificate Of Compliance = a formal document issued by supplier stating that he built the goods meeting Selcom, statutory and regulatory requirements, as well as meeting his own requirements and best-practice know-how.

- REACH = a regulation of the European Union concerning the Registration, Evaluation, Authorization and restriction of CHemicals, adopted to improve the protection of human health and the environment from the risks that can be posed by chemicals. Refer to Regulation (EC) No.1907/2006 of the European Parliament and of the Council of 18 December 2006, in the last consolidated version, including all subsequent applicable amendments (see: http://echa.europa.eu/web/guest/regulations/reach/legislation).

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

1.2. Documents layout

The present TQR document describes Selcom requirements for manufacturing, quality and delivery of bare PCBs. The document and the requirements stated herein apply to all PCBs ordered by Selcom, unless different written instruction from Selcom.

To set forth the supply conditions and the technical production & acceptance parameters of double-side and multi-layer PCBs purchased by Selcom, it is mandatory to know two main files, which are:

1. "TQR-SEL-Rev nn" (where *nn* is the revision number of file), in the following simply referred as "TQR", it is a collection of standard general supply specifications and of other Selcom general rules & policies about PCBs.

2. "MA-pcb ref-Rev mm" (where *pcb ref* is a reference to the part number of PCB, and *mm* is the revision number of file), in the following simply referred as "MA" or "MA file", is a package of files including gerbers and a collection of customized and detailed tech requirements specific for each part number, called "MA documents".

MA file always refers to a specific part number.

Revision index of MA file is independent from revision of part number which refers to.

If Selcom changes a detail just in some document into MA file (for example the surface finishing), the MA file will get an updated revision index even if the gerber files of that part number could not change.

On the other hand, if instead Selcom changes the gerber files there will be anyway an update of revision index of related MA file.

In each Purchase Order, for each part number Selcom will mention name and revision of MA file to use. Should supplier miss such detailed information, he shall ask it to Selcom.

Last revision issued of TQR document shall be checked by supplier on Selcom website:

http://www.selcomgroup.com/SuppliersTechnicalRequirements

Should you need TQR file, ask it to Selcom Group Purchase Dept.

For each Purchase Order, it is mandatory for the supplier to check and follow the documents revisions shown; in case of doubts or any potential anomaly, supplier must ask specific instructions to Selcom Procurement Dept.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

2. GENERAL REQUIREMENTS

2.1. Acceptance criteria

Selcom puts out to contract the building of PCBs to Supplier. The taking over of the goods by Selcom warehouses does not represent an acceptance act, and shall take place as "goods subject to control".

PCBs referring to current specification must be processed in such a manner as to be uniform in quality and technology. PCBs must be free from any other defects than those specified in this document. Statistical process control method must be in place to ensure production quality and respect of Selcom requirements.

Any defective pieces will be scrapped and could cause the rejection of the entire batch, in compliance with the reference specifications listed in current document.

Selcom reserves the right to carry out any test, even only partially, upon receiving the pieces. Selcom has the faculty to perform or to not perform the incoming inspection of PCBs, so as to issue and update related specific operating instructions, conforming to what stated in supply specifications.

Sampling quantities for further tests will be decided according with UNI ISO2859-1 dated January 1993, simple sampling plan for ordinary test, Level (II), and AQL shown in the following:

- ➔ Safety defects (e.g.: board reliability, etc.):.. AQL = 0 (ZERO)
- ➔ Major defects (e.g.: function, dimensions, etc.): .... AQL = 0,1
- ➔ Minor defects (e.g.: appearance, packaging, etc.): .... AQL = 0,25

Even if the overall batch passes the possible tests performed on sampled quantities, every quantities of circuits that turn out to be defective due to defects of PCB, are to be reimbursed by the PCB supplier. In these events Selcom is entitled to claim reimbursements also for all production and materials costs borne up on the scrapped electronic boards/apparatus due to defective PCBs; and also for all economic damages due to production slow-down, production stops, recalls, missed gains, fines, and so on. PCBs could be used in Selcom automated lines running 24 hours/day.

Subject to the acceptance criteria outlined in Selcom specifications, if a batch is to be rejected, Selcom has the right to decide whether or not to accept the batch in partial or total derogation, or to perform partial or total sorting and/or rework in case that urgent production needing arise and PCB supplier is unable to replace/rework the rejected pieces in due time. In some particular cases, a 100% test of the pieces can be performed to check the parameters out of specification, with the aim to possibly use the acceptable part of a batch. In any case, all expenses borne by Selcom for above mentioned activities, will be at supplier's charge.

Should the batch be returned to supplier, the shipping expenses will be at supplier's charge; then - upon request of Selcom Purchase Dept. - supplier will be committed to replace the missing quantities at his charge as soon as possible and within the required time.

Any possible rework/modification/sorting of returned goods shall be agreed with Selcom Quality Dept. before they are performed. Any related permission released by Selcom does not represent in

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

any way an acceptance nor sharing of responsibility from Selcom side about the actions performed by supplier.

2.2. Quantities

The quantities and the acceptable quantity tolerances (plus or minus) are to be agreed with Purchase Dept, unless already specified in purchase orders.
Any shipments containing quantities exceeding agreed tolerances must be authorized beforehand.
The unauthorized excess quantities might be withheld or rejected and the shipping return costs will be at supplier's charge.
Should the quantity be less than the minimum quantity agreed upon, the order will not be considered carried out and the supplier will have to balance the amount within the shortest technical time required.
Excessive fragmentation of shipments must be avoided.

2.3. Supply approval

Supplier must homologate the PCB and its complete production process, including written description of all production phases, site of production, and all raw materials used.

In detail, PCB supplier shall declare BRAND and exact MODEL of the following raw materials:

- **laminates, copper, prepregs;**
- **solder resist ink;**
- **silkscreen (legend) ink;**
- **silver paste;**
- **copper paste;**
- **carbon paste;**
- **undercoat ink;**
- **overcoat ink;**
- **via holes filling resin/ink;**
- **OSP finishing chemicals;**
- **HASL alloy composition;**
- **peelable ink.**

including any eventual alternative (if not otherwise stated in MA file, up to three choices are possible for each material). For all materials proposed, send related full data-sheets to Selcom.
These documents (process flow, list of materials, data-sheets) must be sent by email to Selcom and shipped together with the first samples which Selcom will use for own approval process. See also TQR §8.5.

The supplier, promptly and before building the affected supply, must request to Selcom written approval for any changes of approved production process; production site; materials and/or equipment used.

If supplier wants to add a new material to the approved list, it must issue a written request and wait for Selcom written approval.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Selcom could ask to supplier to send some free-of-charge samples made with new material, to perform new product approval process.

As traceability must always be guaranteed, within the same date-code the supplier must use only one kind of each approved material and must follow the same revision of MA file.

2.4. Documentation

Any physical Selcom documentation (e.g. photographic films) sent to PCB supplier will always belong to Selcom and has to be returned to Selcom in whole and under perfect conditions as soon as possible upon request.

Any Selcom document or PCB built upon Selcom documents is to be considered as strictly confidential and must not be disclosed to any other people or Company, unless prior duly and formally authorized by Selcom in written form.

2.5. No Transfer

The supplier is committed not to transfer orders received by us to third parties.

Furthermore, the supplier is committed not to transfer, or delegate in any way, the credit resulting from supplies carried out.

2.6. Prices

The prices of the supply are those indicated on the purchase order form.

Any difference has to be notified upon order receipt.

2.7. Guarantee of quality

The supplier must guarantee the homogeneity of the supply batch, understood as being both the quantity of boards delivered simultaneously to our storehouses and the batches delivered successively once the first supply has been approved.

The supplier guarantees that he/she has put into effect all the procedures deemed necessary (process checks, in-house tests, etc.) to ensure that all the characteristics of the delivered material are conform to the specifications or documentation received.

Every production batch must be identifiable on each unit piece and must include all documents required in TQR §8.4; §8.5.

All suppliers shall take the necessary risk-management-precautions to ensure a continuous supply to Selcom and avoid business disruptions. These measures include for example: fire extinguishing systems, redundant equipment, safety stocks, disaster recovery plans, etc.

2.8. Oldest acceptable batch

In order to prevent excessive fragmentation of shipments and delivery of PCB batches with inadequate residual shelf-life, Selcom will NOT accept pieces having date-code older than 11 weeks since supplier's shipping date, unless the shipment of those batches was held/delayed on specific written request by Selcom Purchase Department.

In case of a derogation request from supplier (always needed also in case the batch shipment was held by Selcom Purchase Dept.), be noted that Selcom does NOT require nor encourage supplier to automatically perform any preliminary baking or other conditioning/reworking on finished PCBs that have been promptly and always kept well sealed into their original proper packaging and that are still within their original shelf-life (see also §8.3.1).

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

2.9. Documents priority order

The following document priority decreasing order must be applied by supplier:

1st : ***Purchase Order.***
2nd: ***Specific customized PCB documentation (MA documents).***
3rd : ***Technical requirements written as text into gerber files.****
4th: ***The present general technical specification (TQR document).***
5th : ***Related PCB industry standards and other applicable documents, as listed in TQR §2.10 .***

In case of difference between these and other specifications, the supplier must immediately contact Selcom to clarify the specification to follow.

In case supplier knows specifications of final customer of Selcom and notices some conflict with Selcom documents, then supplier shall contact Selcom to get a written instruction.

****note:*** original gerbers made by Selcom's Customers could include some tech requirements written as text, which typically are commented into MA documents. Supplier shall take care that no misunderstandings are left in place, immediately asking Selcom for any possible clarification, in case.

2.10. Applicable documents

If not otherwise specified, following documents are meant in the latest revision issued, inclusive of related amendments.

IPC-A-600	Acceptability of Printed Boards
IPC-601x – Series *(e.g.: IPC-6011; IPC-6012; etc.)*	Qualification and performance specifications for Printed Boards
IPC-2615	Printed Board Dimensions and Tolerances
IPC-4101	Laminate / Prepreg Specification for Printed Boards (CEM1 included)
IPC-4104	Specification for High Density Interconnect (HDI) and Microvia Material
IPC-455x – Series *(e.g.: IPC-4552; IPC-4553; etc.)*	Specifications for Surface Finishings of Printed Circuit Boards
IPC-4562	Metal Foil for Printed Wiring Applications
IPC-TM-650	Test Methods Manual
IPC-SM-840	Qualification and performance of permanent polymer coating (solder mask) for printed board
UL-94	Standard for Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
UL-796	Standard for Printed Wiring Board
IPC-1601	Printed Board Handling and Storage Guidelines

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

IPC-7711/7721	Repair and Modification of Printed Circuit Board and Electronic Assemblies
IPC-9252	Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-7095	Design and Assembly Process Implementation for BGAs
PGR-SEL	Selcom Packaging General Requirements *
BCR-SEL	Selcom Bar-Code Requirements *

(= Last revision issued shall be checked and downloaded from Selcom website at:*

http://www.selcomgroup.com/SuppliersTechnicalRequirements)

2.11. UL marking

See MA file to check requirement about UL marking.
Supplier shall be formally fully enabled by UL to apply markings required in the following.

- **If UL marking is explicitly required**, each single PCB piece must show the following marks and codes:
    - *UL flammability class;*
    - *PCB supplier trademark logo as known by UL **(do not show UL number or other information!)**;*
    - *UL type designator (according UL-card);*
    - *UL mark:* c UL us
    - *When MA file includes a min CTI requirement, and if supplier UL-type-designator on UL-card shows an asterisk sign on the CTI column, then Comparative Tracking Performance Level Category shall be marked on PCB. Syntax is "CTI: PLC n", where "n" shall be conforming to (or better than) CTI requirement shown in MA file. See also §1.1.*

- **If UL marking is explicitly NOT required**, then any supplier identification symbol or mark (apart those required by Selcom lot coding in MA file) is NOT allowed on single pieces; anyway they can be put on breakaways only.

- **If no explicit information is found about UL marking**, please contact Selcom to get a written instruction.

See also §8.1.

2.12. FIFO production logic

Supplier has to ensure that produced PCBs are traceable backwards to his production orders and the related quality and process data. A good traceability can save a whole business and spare a huge amount of issues!

The premise of a good traceability is that the production plan correctly works with FIFO logic ("FIFO" = "First In, First Out").

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

That means that supplier must:

- avoid to process different revisions of Selcom files (MA file) in the same lot-code;
- avoid to process newer lot-codes before have processed older lot-codes;
- avoid to process different lot-codes in the same process shift;
- avoid to process the same lot-code in different process shifts or in different lines/machines;
- implement these actions and all related screenings in its “Process Flow” and “Control Plan” documents.

2.13. All-In-Home processes

Outsourcing some processes (or part of them) is a potential source of defects.

Sub-suppliers are difficult to manage, often don’t know or understand our particular requirements and thus cannot or don’t want to fit their general processes to them; different people with less knowledge manage things; etc… this is why any outsourcing can be a serious source of risks for quality, and then for our whole business relationship.

Selcom strongly encourages supplier to NOT outsource any part of process. For proper discourse, we consider an outsourcing also when processes (or part of them) are made in different plants belonging to the same company or group.

In case supplier wants anyway to outsource something, Selcom must always be fully and preliminary informed about that.

Supplier is responsible for own sub-suppliers, so he will have to perform all actions needed to prevent and survey any quality issue generated by sub-suppliers and related additional handling.

Supplier must receive explicit approval from Selcom before outsourcing any process.

Any sub-supplier automatically becomes part of the global quality supply chain, but remember: no chain is stronger than its weakest ring.

2.14. Scraps and rework policy

Some of our products allow some X-out or some specific simple rework, some other don’t; see MA documents for details. Any rework is source of potential unforeseen defects, whole batches could be rejected because supplier made some apparently harmless rework which instead revealed big side-effect defects after our soldering phase or – even worse – on the final customer application field.

Selcom must be preliminary informed of ANY rework not already foreseen by our specifications.

Selcom reserves its right of discretionally refusing reworks that could lead to quality issues.

If rework is allowed by Selcom (see also TQR §2.1 rules), reworked pieces must be delivered in a separate and identified packaging marked as “Reworked pieces”.

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Panels containing scrap pieces must be delivered in a separate and identified packaging marked as “Panels with scrap pieces”, and with an attached document clearly explaining the nature of scraps.

As a general requirement, we strongly encourage supplier to reduce its scrap ratio and rework needs by means of its technical continuous improvements and strong reduction of handling. It is nonsense for a supplier to invest money and resources in improving its rework capabilities!
That means scraps must be PREVENTED, not repaired!
Then, rework stations should be reduced, with the aim of removing most of them.

2.15. Country of Manufacture

Remove on Selcom gerber files any label indicating the country of manufacture if it does not correspond to the nation of PCB supplier. (e.g.: if on gerber files there is the label "Made in Italy" and the PCB is produced in China, remove the label "Made in Italy").

2.16. Files modifications by supplier

Any minimal modification of COPPER gerber files performed by supplier (even if typical or believed to be necessary to produce boards or to fit selcom's requirements) must be formerly written approved by Selcom!

When board is multiplied in panel, if not otherwise specified (see panel gerber drawing), do not rotate or mirror original gerber files.

For other gerber files, some self-modifications are allowed, examples:

- ➔ Solder mask vias treatment (see TQR §6.4);
- ➔ Solder mask openings around pads (see TQR §6.3);
- ➔ Lot-code and other markings (see TQR §2.11; §8.1 and MA file);
- ➔ Silkscreen (see TQR §6.6);
- ➔ etc...

Anyway, finished PCB shall comply with Selcom Specifications.
Any possible marking possibly required by Selcom gerber files or drawings may be applied by supplier on bare PCB only if allowed by own current qualifications and certifications.

In case of any minimal doubt, supplier shall ask Selcom written confirmation.

Selcom appreciates and strongly encourages supplier's written Engineer Queries preliminary to production; that is the most appropriate moment in which clarifying doubts, and proposing alternative materials and solutions if profitable and applicable. Possibly join all Engineer Queries and related pictures in one single file.

2.17. Test coupon layout

If test-coupons are present in gerber panel drawing, **DON'T** remove non-connected pads and non-connected-traces from inner layers of test coupons. Any doubt, ask Selcom confirmation

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

2.18. Netlist file

When available, alternative-netlist-file supplied by Selcom (e.g.: ODB++; X2 gerber; etc.) SHALL be used to double check production of PCB and related tools.

Examples of alternative-netlist-file uses which PCB suppliers shall perform:

- to find possible errors in Selcom original gerbers;
- to verify congruency of own working gerbers with original Selcom gerbers;
- as a reference for each test based on a comparison with the original Selcom electric diagram. For example: e-test performed by PCB supplier shall be based on Selcom alternative-netlist-file or on an internally developed netlist with same meaning, 100% checked as matching with Selcom one.

Note: Selcom software is able to generate alternative-netlist-file but is unable to use it to validate own mastering activities with full control. For this reason, Selcom alternative-netlist-file shall NOT be meant as a substitute of gerber files! Selcom gerber files shall be used for PCB production; while Selcom alternative-netlist-file is meant to be used only for the above mentioned checkings.

When alternative-netlist-file is not supplied by Selcom, PCB supplier shall generate own netlist file from Selcom original gerbers, and shall use that netlist to perform all the above mentioned possible verifications and checkings.

3. GENERAL MANUFACTURING SPECIFICATIONS

3.1. Base materials

For all raw materials listed in TQR §2.3:

a) when no specific approved raw materials are listed in MA file, PCB supplier is responsible for choosing the best appropriate raw materials (showing exact brand/model names), given the final customer application and all the technical features of PCB;

b) PCB supplier must define proposed raw materials list (as per TQR §2.3) BEFORE homologation phase, and obtain Selcom written approval before their usage in any production;

c) PCB supplier cannot change approved raw materials unless further written approval got from Selcom;

d) PCB supplier cannot use different raw materials in the same batch of PCBs;

e) every technical and/or chemical changes in raw materials must be notified to Selcom, even if part number of involved raw materials does not change.

Upon the PCB being finished, no manufacturing defects must be noticeable on the material, such as: weave texture/exposure, delamination, measling, crazing, haloes, and stains.

Furthermore, burnout and/or excessive changes of color of any raw material after standard Selcom soldering/manufacturing processes, are not tolerated. In any case rolled section defects are to be evaluated conforming to the IPC-A-600 Standard (ref. TQR §2.10 for revision).

ALL LAMINATES USED MUST BE OF PERFECT CHECKED QUALITY AND WELL STABILIZED (if necessary through a preliminary baking/pressing session on raw laminates) to be sure of:

a) have removed any excess of internal humidity;

b) have relaxed and discharged any internal mechanical tension forces, so to prevent any excessive bow&twist issues on finished PCBs.

“FR4” materials used for manufacturing of the printed circuits must be conforming to "IPC-4101", "nema LI-1" or "IEC 249" Standards with a “V0” class of inflammability.
Selcom prefers base materials with “CAF resistant” features.

In not otherwise specified in MA file, CTI minimum required value is 175 Volts.

For standard raw materials, PCB suppliers shall choose only worldwide notorious trademarks as per the following Selcom preferred list (in mixed order):

- NanYa (http://www.npc.com.tw)
- Kingboard (http://www.kblaminates.com/)

- Shengyi (http://www.syst.com.cn)
- Panasonic (http://www.panasonic-electronic-materials.com/) Panasonic
- Iteq (http://www.iteq.com.tw)

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

- Isola (http://www.isola-group.com/) isola
- EMC (http://www.emctw.com)

- Doosan (http://www.doosanelectronics.com)

- Chang Chun (http://www.ccp.com.tw)

- Grace (http://www.graceepoxy.com)

Original raw-material-maker identification trademark shall always be applied on raw material, regardless from its thickness.

3.2. Dimensional Requirements

If not otherwise specified in MA file or master drawing, the following tolerances have to been kept *(ref. ISO 2768m)*:

Dimension	Tolerance
L ≤ 6,00 mm	+/- 0,1 mm
6,00 < L ≤ 30,00 mm	+/- 0,2 mm
30,00 < L ≤ 120,00 mm	+/- 0,3 mm
120,00 < L ≤ 400,00 mm	+/- 0,5 mm
400,00 < L ≤ 1000,00 mm	+/- 0,8 mm

Unless otherwise specified in MA file, the requirement about final total thickness/tolerance of finished PCB has priority over the sum of thicknesses and tolerances of single layers shown in the Build-Up.

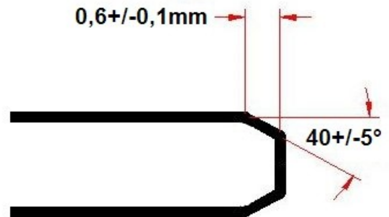
Other typical mechanical tolerance in following table:

Dimension	Tolerance
Routed shape to reference hole:	+/- 0,15 mm
Punching shape to reference hole:	+/- 0,15 mm
Sawing shape to reference hole:	+/- 0,15 mm
Alignment printing processes to reference hole (e.g.: Carbon, marking, peelable ink, etc.):	+/- 0,15 mm

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Dimension	Tolerance
Alignment between fiducial mark and reference holes:	Conductive pattern by: • photo resist: +/- 0,1 mm • screen printing resist: +/-0,2 mm
Alignment between Copper pads and between Copper pads and fiducial marks (also called "Copper pattern shifting"):	• Dimension ≤ 187,5 mm: +/- 0,075 mm • dimension > 187,5 mm: +/- 0,04 %

Unless otherwise specified in MA file, dimension of chamfer (where required) shall be:



3.3. Holes dimension and tolerance

If not otherwise specified in the drilling table or elsewhere in MA file, the standard diameter tolerances are the following:

Dimension	Tolerance
Diameter of non-plated drilled holes	*Nominal dimension -0,00 / +0,10 mm*
Diameter of plated drilled holes (except press-fit holes)	*Nominal dimension -0,05 / +0,10 mm*
Diameter of plated press-fit holes (if present they are indicated in drill table):	*Nominal dimension -0,05 / +0,05 mm*
Dimension of non-plated slots (milled / punched)	*Nominal dimension -0,10 / +0,10 mm.*
Dimension of plated slots (milled / punched)	*Nominal dimension +0.10 / -0.05 mm in width direction* *Nominal dimension +0.10 / -0.10 mm in length direction*
Distance between holes	*Nominal dimension -0,10 / +0,10 mm*
Distance between slots centers	*If nominal dimension ≤300 mm: +/- 0,07 mm* *If nominal dimension >300 mm: +/- 0,10 mm*
Roughness of drilled hole walls	*Max 25,4 µm from "max peak" to "min valley" of same drilled hole wall.*

Tolerances on holes diameter include also conical shape errors and drilling defects.
All the holes (plated and not-plated) must be drilled in the same single phase.
For copper plated holes, diameters indicated in gerber files refer to finished holes (after plating).
For STH or CPTH holes, diameters indicated in gerber files refer to drilled holes (after drilling).

3.4. Warping and twisting

A maximum warping and twisting limit of 0,75 % is allowed on finished PCB if the distortion is homogeneously distributed on the whole PCB surface (if the warping and/or twisting insists only on a limited portion of the panel, acceptance limit could be lower than what above mentioned).

For flexible and rigid-flex PCBs, bow&twist requirements apply only to the rigid parts of it (e.g.: stiffener; etc.).

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

For the measurement of bow&twist, apply the methodology of the IPC-TM-650, §2.4.22e.

Damaged anchorages are anywhere unacceptable, even if originally flat against bare pcb surface (damage can cause panel bending during Selcom normal production process).

Any modification of gerber files necessary to prevent and reduce bow&twist issues must be proposed to Selcom as soon as possible before production of PCB.

Base materials shall be preliminary checked and stabilized by supplier, as requested in TQR §3.1. Any cost sustained by Selcom to rework finished PCBs showing anomalies (e.g.: excessive bow or twist; blistering after soldering, etc.) during their usage within their expiration date, will be charged to supplier. See TQR §2.1 for further details.

3.5. V-cut (scoring)

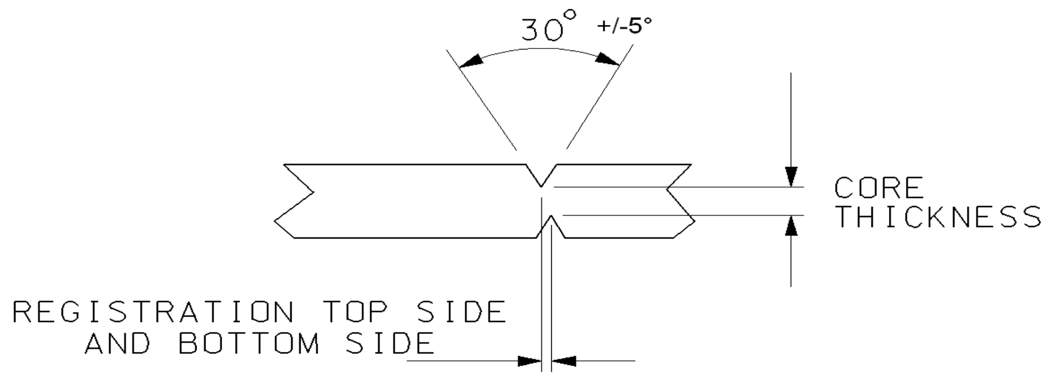
When V-cut is required, the incision angle of scoring must be 30 degrees unless otherwise specified.

After scoring, following core thickness is required unless otherwise specified:

Nominal Board Thickness	***Core Thickness after scoring***
≤ 1.2 mm	*0,4 +/- 0,1 mm*
> 1.2 mm	*0,5 +/- 0,1 mm*

Scoring line position tolerance: +/- 0,1 mm

Edge to reference hole: +/- 0,15 mm



maximum allowed mis-registration between top side and bottom side lines: 0,15 mm.

3.6. IPC-A-600 minimum requirements

The IPC-A-600 class of PCB is specified in MA file (if not specified, assume Class 2 as default).

If MA file does not specify a higher IPC class, for the following items the minimum listed requirements of IPC-A-600 shall be met:

IPC-A-600 chapter	IPC-A-600 paragraph	Additional requirements	Min Class required
Base material subsurface	Crazing	- - -	2
Base material subsurface	Delamination/Blister	- - -	2

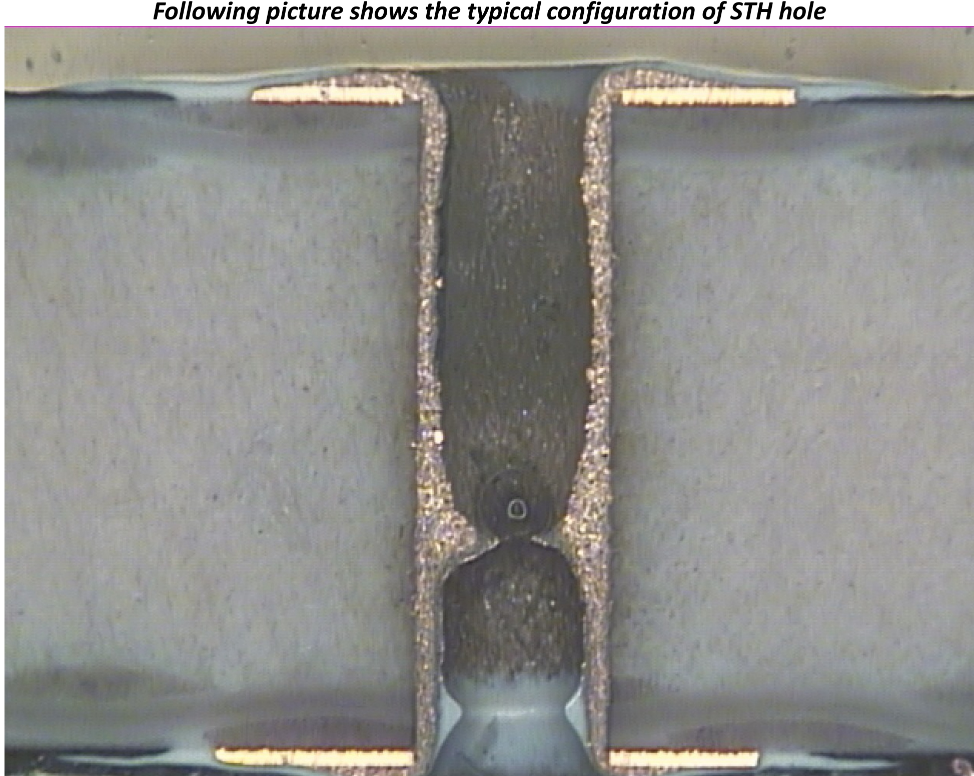
 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

IPC-A-600 chapter	IPC-A-600 paragraph	Additional requirements	Min Class required
Solder coatings and fused tin lead	Dewetting	- - -	2
Holes- plated-through - general	Voids - Copper Plating	See TQR §5.2	3
Holes- plated-through – general	Voids - Finished Coating	- - -	2
Printed contacts	Surface Plating - General	- - -	2
Solder resist (Solder mask)	Coverage Over Conductors (Skip Coverage)	- - -	2
Solder resist (Solder mask)	Blister / Delamination	- - -	2
Solder resist (Solder mask)	Adhesion (Flaking or Peeling)	see TQR §6.3	3
Solder resist (Solder mask)	Coverage over conductors (Skip Coverage)	- - -	2
Solder resist (Solder mask)	Soda Strawing	- - -	3
Dielectric material	Laminate Voids (Outside Thermal Zone)	- - -	2
Dielectric material	Delamination/Blister	- - -	2
Pattern definition – dimensional	Conductor Width	see TQR §4.2	2
Pattern definition – dimensional	Conductor Spacing	see TQR §4.2	3
Pattern definition – dimensional	External annular ring – Supported Holes	see TQR §4.1	3
Pattern definition – dimensional	External annular ring – Unsupported Holes	see TQR §4.1	3
Plated-through holes – general	Annular Ring – Internal layers	Annular ring shall be greater than zero	2
Plated-through holes – general	Foil crack – (Internal Foil) “C” Crack	- - -	2
Plated-through holes - general	Foil crack – External Foil	- - -	2
Plated-through holes – general	Plating Voids	Plating voids are not acceptable. See also TQR §5.2	3
Plated-through holes – general	Wicking	- - -	3
Plated-through holes – general	Wicking, Clearance holes	minimum clearance >50 % of dimensional requirements. minimum absolute = 3,5 mils	3
Plated-through holes – general	Innerlayer Separation – Vertical (Axial) Microsection	- - -	2
Plated-through holes – general	Innerlayer Separation –Horizontal (Transverse) Microsection	- - -	2

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

3.7. Silver-Through-Hole technology

Following picture shows the typical configuration of STH hole



STH process performed by PCB supplier must be able to withstand lead-free soldering processes (if not otherwise specified on MA file, 3 consecutive lead-free reflow or wave soldering cycles).

Standard one-component-heat-curing homologated silver pastes are the following:
- ➔ FUJIKURA KASEI, models: “FA-545” or “FA-510” or “XA-1088”.

Any new silver paste type could be used only after getting written approval from Selcom (see TQR §2.3).

Typical STH resistance (measured on finished bare PCB): within 50 x 10^{-3} Ohm/hole

All following requirements shall be met for each STH hole:
- ➔ Resistance measured after homologation tests: maximum 100 x 10^{-3} Ohm/hole
- ➔ Resistance measured after all soldering processes: maximum 100 x 10^{-3} Ohm/hole
- ➔ Minimum insulation resistance between any two via holes: 100 x 10^{6} Ohm
- ➔ Rated current max continuous DC loading:
  - ➔ 300 mA/hole (for FR1 material);
  - ➔ 500 mA/hole (for CEM1/CEM3/FR4 base materials).
- ➔ Power surge DC current: 1 A/hole (5 seconds)

Note: “maximum” or “minimum” are meant as statistical limits to be evaluated with the most appropriate mathematics statistical distributions, and to be fit within 50 ppm.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

3.7.1. Requirements of STH Construction

Fig.1

Ring of Silver Paste

Top Side

Cover Coat

Copper Foil

Laminate

Silver Paste

Solder Mask

Copper Ring

Bottom Side

Fig.2

Silver-print side
= SMD components side

A1

B1

A2

B2

C1

D

B1

A3

B2

C2

F

Silver-nonprint side

Fig.3

H

G

Copper Ring

Silver Ring

Overcoat (dashed area)

Center void of overcoat
(ventilation hole)

Ventilation hole is needed at least on print side.
Overcoat must completely cover silver land; only on inner silver ring it is allowed a silver exposure not greater than 20 % of silver land area.

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Item	Description	Specification	Other Requirements
A-1	Silver Thickness (Corner)	MIN 10 µm	No cracks or separations in the hole.
A-2	Silver thickness (Print side)	MIN 10 µm	
A-3	Silver thickness (Nonprint side)	MIN 20 µm	
B-1	Overcoat thickness over copper (Print side and Nonprint side)	MIN 4 µm on conductor edge	see Fig.2
B-2	Overcoat thickness over silver (Print side and Nonprint side)	MIN 4 µm; MAX 40 µm	
C-1	Overcoat+Silver thickness (Print side)	MAX 50 µm	- - -
C-2	Overcoat+Silver thickness (Nonprint side)	MAX 80 µm	- - -
D	Separation of silver paste from hole wall	Not allowed.	- - -
E	Ring of silver paste minimum diameter	Print and Nonprint side: 0,10 mm	Resistance of STH within specification.
E	Ring of silver paste maximum diameter	Not larger than the size of copper ring.	
F	Drilled hole	MIN diam. 0,5 mm	Tolerances as per §3.3, non-plated holes
G	Overcoat land diameter	= copper pad diam.+ MIN 0,6 mm	see Fig.3
H	Overcoat ventilation hole	MIN diam. 0,04 mm	

3.7.2. Copper-Paste-Through-Hole technology

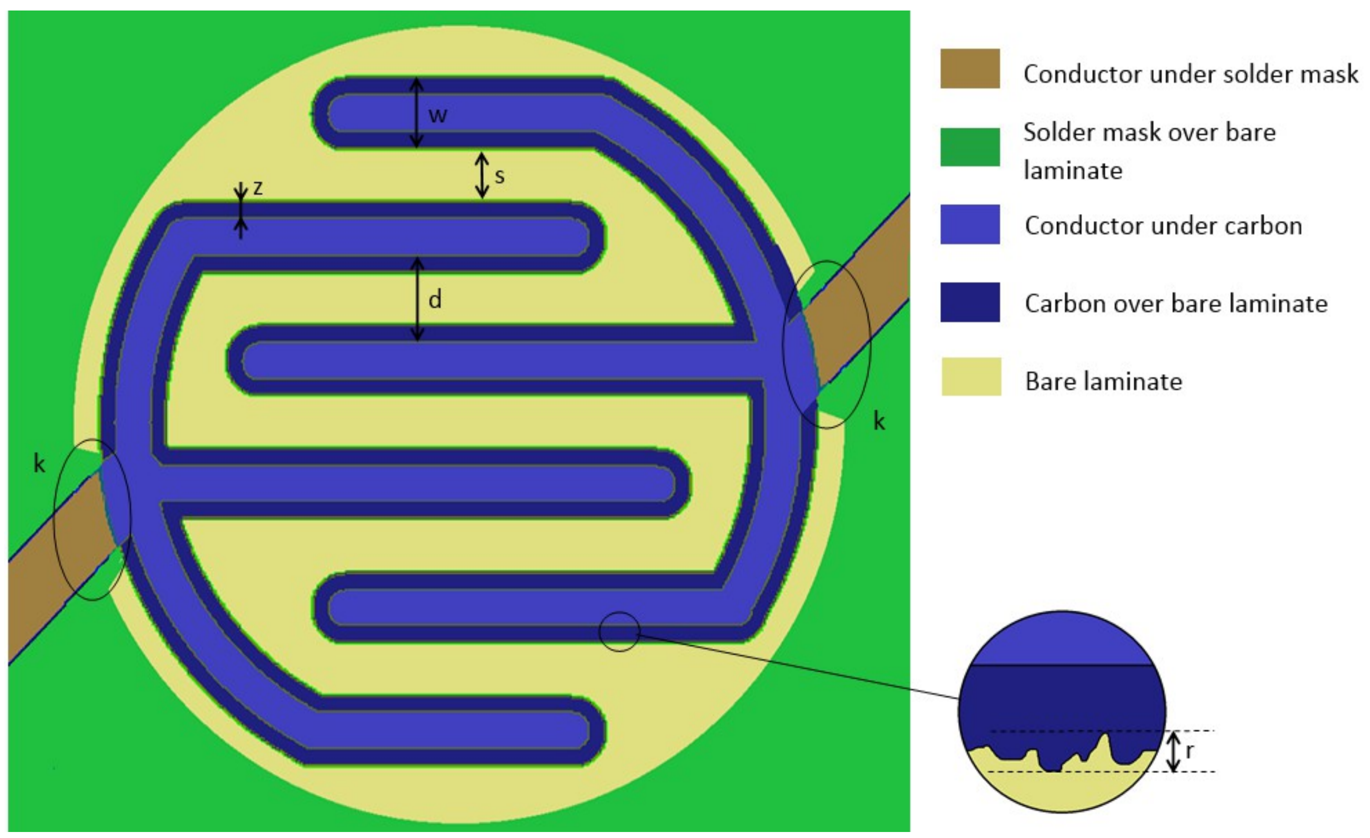
Specifications required for Copper-Paste-Through-Hole (CPTH) technology are the same listed in §3.7 and §3.7.1 for STH technology, with the following modifications:

- ➔ "STH" acronym is replaced by "CPTH" acronym;
- ➔ "silver" and "silver paste" words are replaced by "copper paste" words;
- ➔ in spreadsheet §3.7.1, item “F: drilled hole MIN diameter” is 0,4 mm;
- ➔ HOMOLOGATED COPPER PASTES:
  Preferred (for surface finishings: OSP, HASL, HASL-LF): HARIMA CP-700.
  Alternatives (only for OSP surface finishing): TATSUTA TH1168FX; TATSUTA TH9968.
- ➔ HOMOLOGATED LAMINATES:
  Preferred: NAN YA CEM-3-92PY.
  Alternatives: NAN YA CEM-3-10; NAN YA CEM-3-01PY; SHENGYI S2600R; CHANG CHUN CCP308C.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

3.8. Requirements for carbon-conductive PCBs

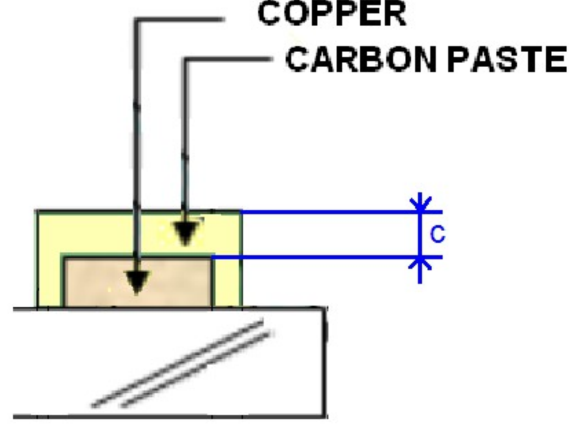
3.8.1. Typical design of carbon contact key pad



Solder mask is typically not required inside carbon key pad area.

Exposed copper or exposed surface finishing is not recommended in the connection areas (above marked with “k”).

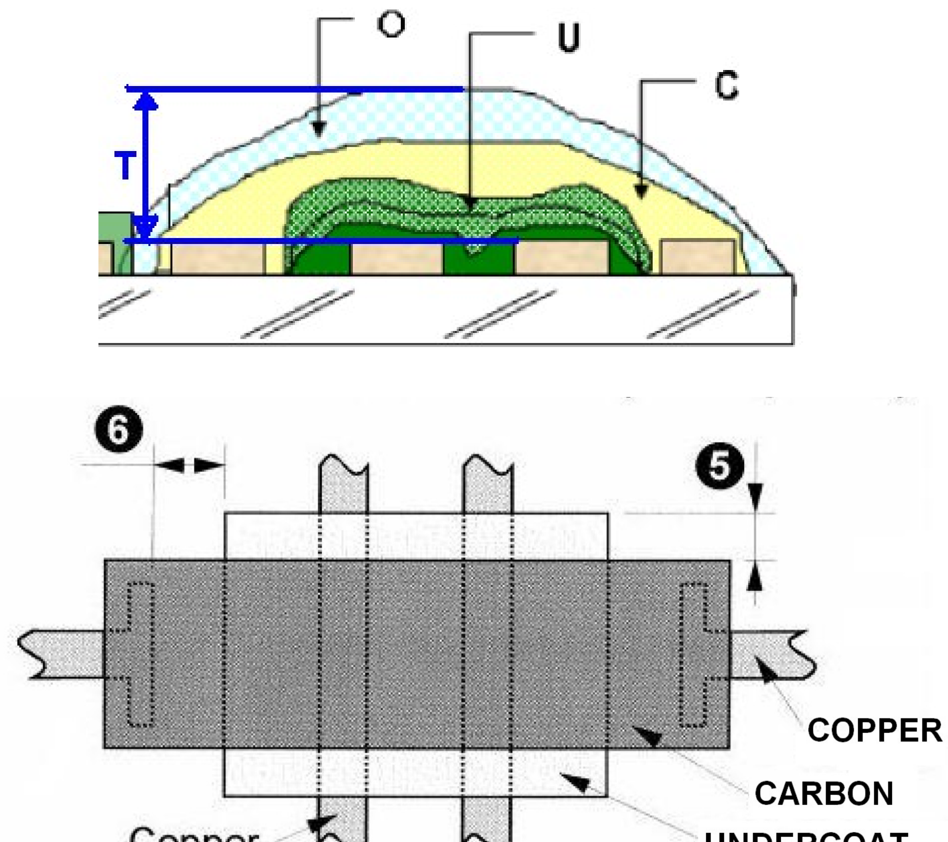
3.8.2. Configuration cross-section of carbon contact



Conductor exposure anywhere not allowed.

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

3.8.3. Configuration design of carbon crossover jumper



3.8.4. Specifications table

Note: symbols used in following table are those defined in pictures of paragraphs 3.8.1; 3.8.2; 3.8.3.

Ref	Description	Typical	Tolerance
w	Carbon width if nominal width ≥ 1,0 mm if nominal width < 1,0 mm	 - -	 +/-0,15 mm +0,20/-0,10 mm
d	Nominal distance between consecutive unconnected conductors	see gerber files	-
s	Spacing between carbon if “d” ≥ 0,5 mm if “d” < 0,5 mm	 - -	 min: d – 0,3 mm min: 0,2 mm
z	Carbon overlap to conductor if ”w” ≥ 1,0 mm if ”w” < 1,0 mm	 - -	 min: 0,100 mm min: 0,075 mm
5	Undercoat (isolation mask) overlap to carbon	-	min: 0,5 mm
6	Distance from copper conductor to undercoat	-	min: 0,2 mm
-	Overcoat (outer protection mask) overlap to carbon or undercoat	-	Min: 0,3 mm per side

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Ref	Description	Typical	Tolerance
r	Carbon edge roughness	-	Max: 15 % of carbon nominal width
C	Carbon paste thickness [1]	20 µm	-10/+15 µm
U	Undercoat thickness	20 µm	-0/+10 µm
O	Overcoat thickness	15 µm	-5/+15 µm
T	Global thickness over conductors level [2]		Max: 95 µm
3.8.1 3.8.2 3.8.3	Carbon aspect on finished PCB	Sharp shaped, good print definition.	-
3.8.1 3.8.2 3.8.3	Adhesion tape test (as per IPC-TM-650 §2.4.1)	-	No detachments left on tape, at any location tested on finished PCB.
3.8.1 3.8.2	Contact resistance of carbon key pad, measured on finished pcb [3]	25 Ohm / pad	-10/+5 Ohm
3.8.1 3.8.2	Contact resistance of carbon key pad, measured at 50±5 kPa after all soldering processes	-	Max: 50 Ohm / pad
3.8.1 3.8.2	Carbon contact resistance variation during life (50±5 kPa x 2 hits/s x 1500000 hits)	-	less than 50 % against original resistance
3.8.3	Carbon sheet resistivity measured on finished pcb [4]	15 Ohm / square	+/- 10 Ohm
3.8.3	Carbon sheet variation after all soldering processes	-	+/- 20 % against original resistance
3.8.1 3.8.2 3.8.3	Insulation resistance (at DC 40V)	-	min: 100 MOhm
3.8.1 3.8.2 3.8.3	Rated DC voltage	20 V	

Notes:

[1] Multiple carbon layers are not allowed. One pass only is allowed.

[2] Conductors level is meant as the outer finished surface of smd pads on the same PCB side.

[3] Using a conductive-rubber button (surface resistance ≤ 10 Ohm/square) shorting at least two thirds of conductive fingers under a total pressure of 50+/-5 kPa.

[4] With carbon layer thickness 20 µm.

3.8.5. Homologated Carbon Inks

Supplier	Model
Asahi	TU-30SK
Henkel	CP-8120
Tamura	MRX-713J-A
Tamura	CLX-204

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

3.8.6. Homologated Over Coating material

Supplier	Model
Tamura	USR-11B
Tamura	USR-2G FY-41-120
Tamura	USR-2G-F24C
Goo Chemicals	PSR-311

4. DIMENSIONAL REQUIREMENTS OF CONDUCTORS LAYOUT

Conductors design width is the width measured on the original 1:1 gerber files supplied by Selcom. Finished track width is measured at the base of the track.

4.1. Minimum annular ring

Minimum admissible condition for external annular rings (see figure below):

For internal annular rings, ref. §3.6 .

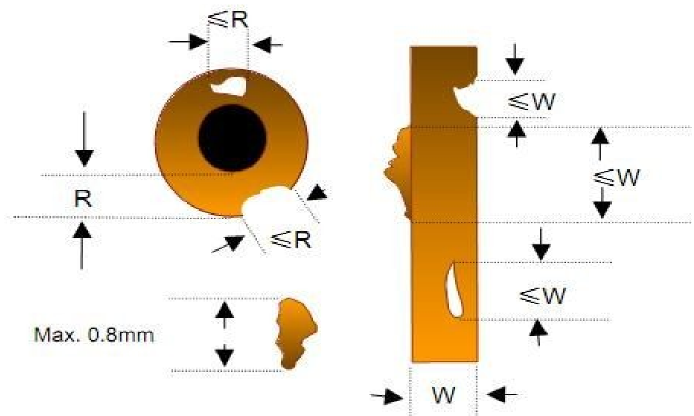
4.2. Width of conductors and insulation

For tolerances refer to ***IPC-6012C §3.5.1; §3.5.2.***

4.3. Conductors imperfections

Localized imperfections (ragging, bunching, nicks, scratches) are tolerated if all below conditions are fit:

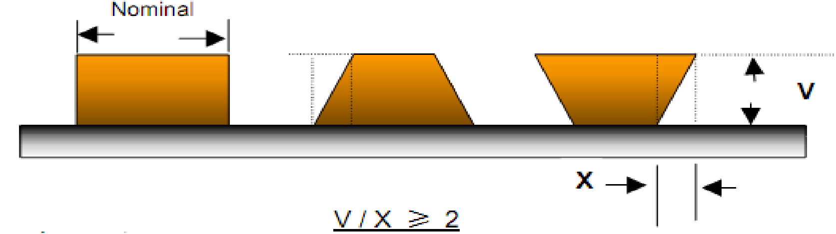
- ➔ any imperfection must not reduce the conductors width or insulation under the limits described in TQR §4.2;
- ➔ imperfections are within a max. quantity of 1 unit every 100 square cm, and no more than 3 units in one side of PCB;
- ➔ imperfections dimension are within the maximum dimensions specified in the drawing below, too:



Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

4.4. Etching

Following conditions must be met:



5. GALVANIC COATINGS

5.1. Etching

The adhesion of any galvanic coatings performed on PCB (copper, nickel, gold, etc) shall pass IPC-TM-650 no.2.4.1 with no detachments left on tape, at any location tested on finished PCB.. The tear test,shall be performed on 3 different points per each side on the printed circuit surface with presence of coatings to test. No coating detachments are allowed as result of this test.

5.2. Copper plating inside via holes

Minimum copper thickness inside via holes must fit requirements of IPC-A-600 Class indicated in MA file.

Maximum copper thickness in a via hole must be compatible with the diameter tolerance of that hole.

The plated holes surface must be homogeneous, without any minimum copper interruption or void.

Any defect on galvanic coating is <u>not tolerated</u>.

The percentage of defects caused from bad plated holes must be zero %.

5.3. Gold plated contacts

When requested in MA file, a thick layer of electrolytic nickel and galvanic gold is requested for PCB contacts or edge connectors.

The Ni/Au plating thickness and purity requested are specified in MA file.

The porosity of gold plating shall be inspected by means of IPC-TM-650 test method 2.3.24.2, Method 3 (§3.3) (or ISO 14647:2000); worst acceptable result is: max 10 corrosion pores bigger than 35 µm (none bigger than 200 µm) in any 2,50 x 1,75 mm area (+/-0,50 mm per side).

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

6. SURFACE TREATMENTS

6.1. Solderable Surface finishing

The finishing requirement of the PCB is specified on MA documents.

The solderable finishing must be applied after the solder resist mask process.

The adhesion of the finishings must be tested in accordance with IPC-TM-650 no.2.4.1, with no detachments left on tape, at any location tested on finished PCB.

Any surface finishing (except OSP) must guarantee that whatever un-solderable Inter-Metallic-Compound does not reach pads surface after 3 consecutive lead-free reflow or wave soldering cycles (or more, if more than 3 soldering cycles are specified in MA file) performed within the shelf life of the batch.

Minimum HASL thickness shall be measured on center of finished solderable biggest pads of the PCB.

Maximum HASL thickness shall be measured on center of the finished solderable smallest pads of the PCB.

If not otherwise specified in MA file, minimum thickness of HASL finishing is not considered as a strict limit; as the priority is that the perfect solderability by Selcom of the finishing shall be guaranteed during all the shelf life of the PCB. However, as basing on Selcom experience the measurement of HASL thickness significantly lower than 1,0 µm brings to a higher risk of solderability issues, when measuring such low HASL thickness Selcom could decide to perform (at supplier's charge) additional tests (also destructive) on some samples in order to further investigate on the alleged solderability of boards before using them (see also par. 2.1). However, any sampling test performed by Selcom does not represent in any way an acceptance nor sharing of responsibility from Selcom side about the actual soldering performance of the whole related batch.

6.2. Wettability

Wettability (or solderability) is one of the most important key features of a PCB, directly affecting the long-term reliability of the final electronic assembled product.

The soldering processes of electronic components on PCBs are often delicate and influenced by a large number of variables; on the other hand PCB suppliers usually have poor experience with soldering, and too rough systems to check wettability (e.g. “dip-in test”); thus the only way for PCB suppliers to release good and reliable PCBs is to perform a perfect production process, with special care about surface finishing and packaging processes.

Wettability can be affected by many different PCB defects; using test coupons and performing other special inspection tests, sometimes it is possible to highlight some wettability weaknesses of PCBs (for example: after being soldered by Selcom, at least 95 % of each pad area must be uniformly covered by the soldering alloy, which must be bright, regular and devoid of oxides), but anyway often the final acceptance of PCB wettability can be assumed only deeply inspecting the soldering joints after have soldered components on PCB.

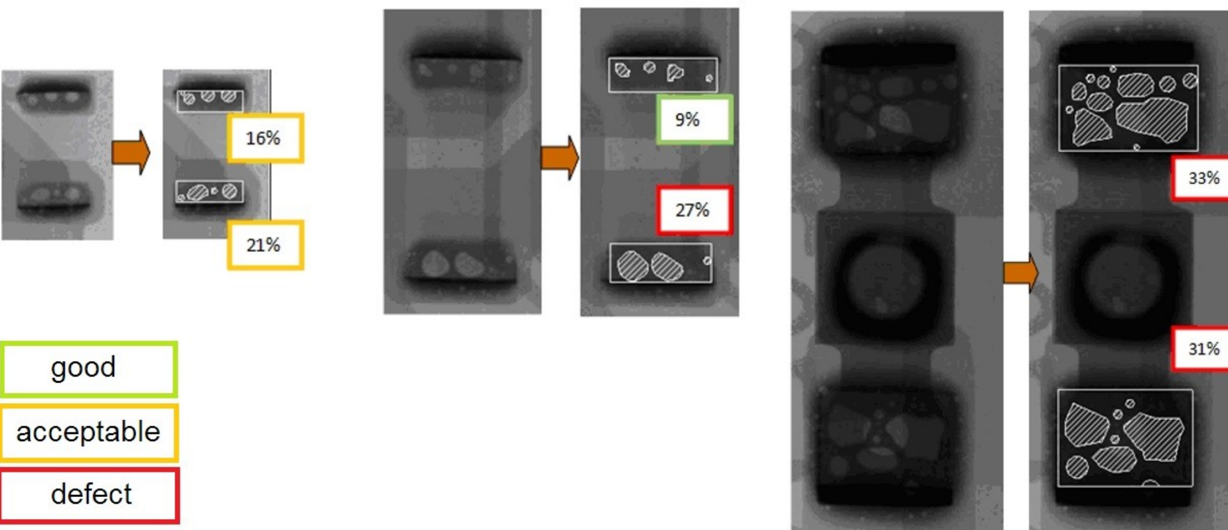
 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Selcom owns a top-level know-how about soldering components onto all kind of PCBs, thus holds the experience and the right to decide whether a PCB batch has enough good solderability or not; being able to show its own standard soldering processes, so as the methods and procedures followed to draw any conclusion.

PCB supplier is intended to accept what above stated; and must preliminary write to Selcom any special instruction required to store PCBs and preserve their wettability (shelf life included, see TQR §8.3).

If not otherwise specified in relevant documentation, PCB could be assembled through lead-free soldering processes.

"Solder voiding" effect (see §1.1) is strongly correlated to perfect cleanness and solderability of PCB pads (see also §6.3 to see the influence of Solder Mask process on solder voiding). If not otherwise specified, voiding is tolerated in solder joints of standard SMD components (non-BGA) when cumulative projected area of all voids under the pin is not greater than 25 % of pin area in a x-ray planar bi-dimensional x-y image, even though supplier should put in place actions in order to reduce it under 10 % target (for BGA components, refer to IPC-7095). See below picture:



6.3. Solder resist protective covering

It is required to apply Solder Mask On Bare Copper (= SMOBC).

The solder resist thickness and tolerances are indicated on relevant PCB MA file.

Unless otherwise specified in MA file, acceptable solder resist thickness at any place on the PCB shall be:

- minimum 5 µm from conductor edges, and above flat conductors;
- maximum 40 µm over flat conductors (in each PCB side with SMD soldering pads);
- on areas without conductors: minimum 5 µm; maximum: lower or equal than total thickness of nearby conductors+solder mask.

The solder mask coating must have an even layer, devoid of dirt or foreign matters, holes, air bells in according with IPC-A-600 standard and exceptions listed in TQR §3.6.

The shape and the dimension of the solder mask showed in the gerber files must not be changed by the supplier, except for solder mask openings around pads (e.g.: SMD, IC-Test pads),

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

that must be expanded from copper sides by 0,10 mm for LPI process and by 0,15 mm for UV process. Anyway it must be secured that a minimum 100 µm wide solder mask dam is always left between adjacent pads. Multiple solder mask coating is not allowed unless explicitly required by relevant specifications (MA file). Any doubt, ask Selcom's written approval.

The adhesion of the solder to the surfaces must be checked by means of test IPC-TM-650 no.2.4.28.1 (supplier shall put related coupon on own working panel breakaways, if not already put by Selcom on delivery-panel breakaways) and shall pass also IPC-TM-650 no.2.4.1 with no detachments left on tape at any location tested on finished PCB.

Hardness of solder mask surface shall be tested as per IPC-TM-650 test no.2.4.27.2; cut-into or gouge the solder mask surface is not allowed under “5H” grade hardness pencil.

Markings required to be realized as openings on solder mask layer shall not expose underlying conductors.

Alignment between fiducial mark and solder mask:

- if with screen printing technology: +/- 0,2 mm;
- if with photo sensitive resin systems: +/- 0,1 mm.

The solder resist shall not cover the pads for components mounting.
Will be accepted PCBs with solder resist apertures tangent to the pads (see picture below).

In order to prevent solderability issues (uneven wettability, excessive “solder voiding”, etc.), supplier shall guarantee that solder resist ink never pollutes pads to be finished. Solder resist shall be completely cured before proceeding to next process steps. Compatibly with the solder-resist-ink used, after normal curing an additional UV curing (“UV-bump”) is recommended to increase chemical resistance of solder mask surface (mandatory requirement before all chemical surface finishings). After Solder Mask process and just before surface finishing process, the contamination level on bare PCB shall be not greater than an equivalent of 0,8 µg/cm^2 of Sodium chloride, measured in accordance with IPC-TM-650, Method 2.3.25, paragraph 4, Resistance of Solvent Extract Method (it should be no more than an equivalent of 0,5 µg/cm^2 of Sodium chloride before chemical surface finishings).

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

6.4. Via holes and solder resist treatment

MA file drives the choice among the following solder resist treatments for via holes. It may happen that some via holes need a different treatment from others in the same PCB; always refer to MA file and gerber files, and ask Selcom all clarification in case of doubts.

Solder resist applied shall be everywhere conform to TQR §6.3.
All vias holes must be completely free from metal alloy residuals or any other kind of dirt/foreign matter, except solder resist where required.

Solder resist inside vias (when allowed) must be completely and properly cured.

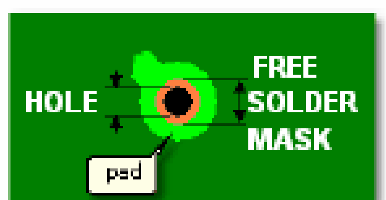
If gerber files of solder mask are different than the "Vias fill requirement" CASE required by MA file, supplier shall ask Selcom written clarification.

When more than one CASE is allowed for a given p/n, supplier shall choose just one of them and then keep it as part of own homologated production process (subject to rules listed in §2.3).

6.4.1. Free from solder mask (CASE 1)

When **CASE 1** is required by MA file, via hole must be free from solder resist.
On finished board, each via hole shall be free from any kind of occlusions and shall let the light freely pass through the whole hole diameter.

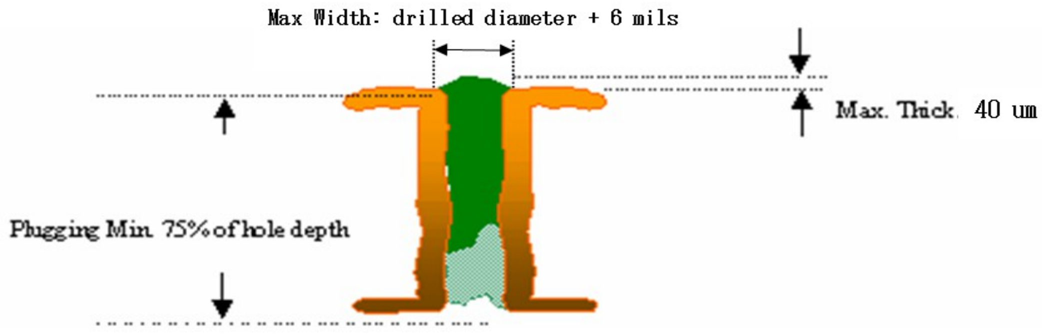
Target: "solder mask free" diameter ≤ "finished hole" diameter + 8 mils



Finished PCB shall be compliant with §6.3 requirements.
Solder Mask opening tangent to hole edge is acceptable, provided that solder ink does not flow into the hole.

6.4.2. One-side plug-in (CASE 2)

When **CASE 2** is required by MA file, via hole must be plugged-in and sealed like in following picture

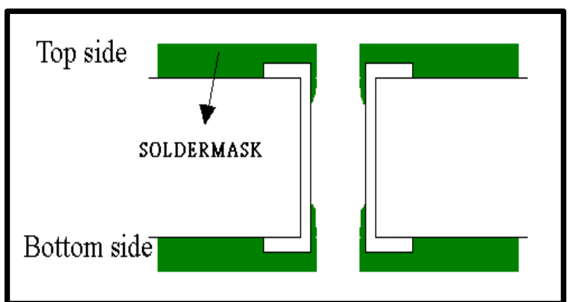


 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

This vias treatment shall be avoided on PCB with chemical surface finishing, except when aspect ratio of finished hole (= finished hole height / finished hole diameter) is ≤ 2 with plugging depth 75%.

6.4.3. Vias corners covered with solder mask (CASE 3)

When CASE 3 is required by MA file, the solder resist shall be applied over via hole corners like in the following picture:



On finished board, each via hole shall be free from any kind of occlusions; light shall pass freely through the hole.

6.4.4. Via fill (CASE 4)

When **CASE 4** is required by MA file, selected vias shall be completely filled-in and sealed with appropriate filling ink, as showed in picture below.

Vias pads on both sides of PCB shall be completely free from solder mask and perfectly solderable.

If not otherwise specified in MA file, homologated via-fill materials are:

- ➔ Peters, VF2467.
- ➔ San-ei Kagaku, PHP900 IR-6P.
- ➔ Goal Searchers Zhuhai, GSH-00400.

Should supplier want to propose a different via-fill material, see instructions at §2.3.

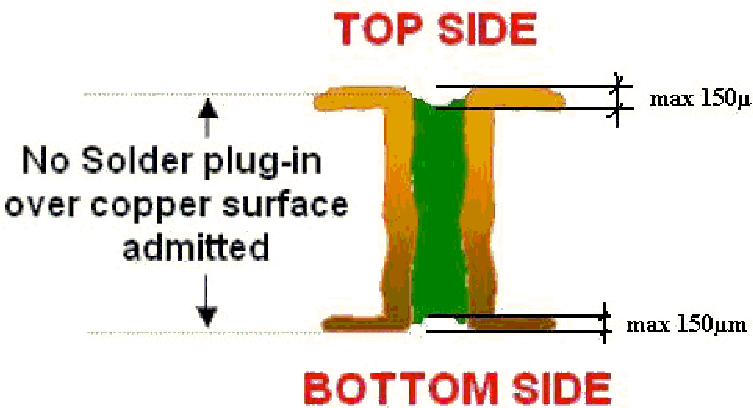


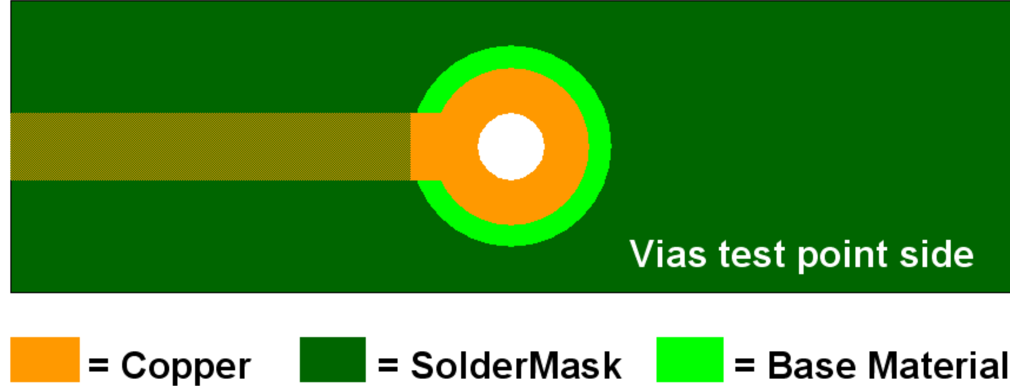
Figure: Soldermask via plug dimensions.

<u>Vias treatment shall withstand with no issues to thermal stress as per IPC-TM-650 2.6.8 (condition A); after test ink voids/cracks/recessions are not acceptable if exceeding 80 μm size or overall exceeding 40 % of via ink-height.</u>

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

6.4.5. Via test-point (CASE 5)

For those vias used as electric-test-points, the final result is showed below:



= Copper = SolderMask = Base Material

Target: solder mask opening diameter on finished pcb ≤ finished pad diameter + 8 mils.

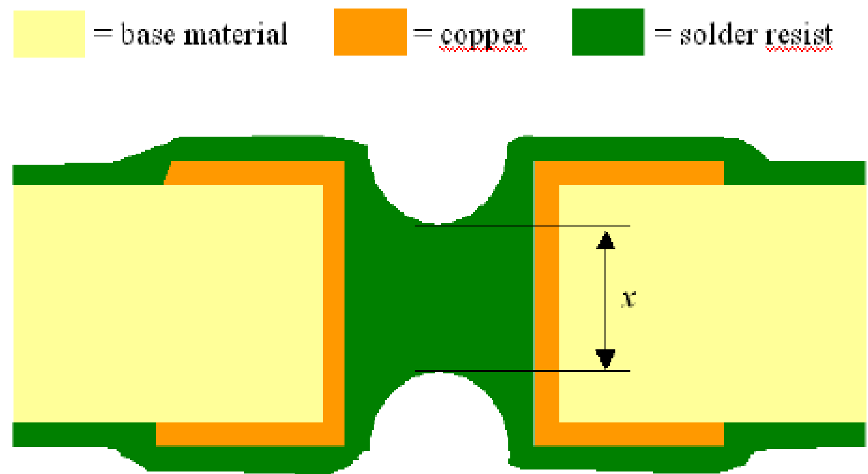
For the vias pad on the side opposite to "Vias test point side", CASE 1 is required. In case of different indications on our files, ask Selcom written clarification.

Finished PCB shall be compliant with §6.3 requirements.

6.4.6. Via hole closed and sealed by solder resist (CASE 6)

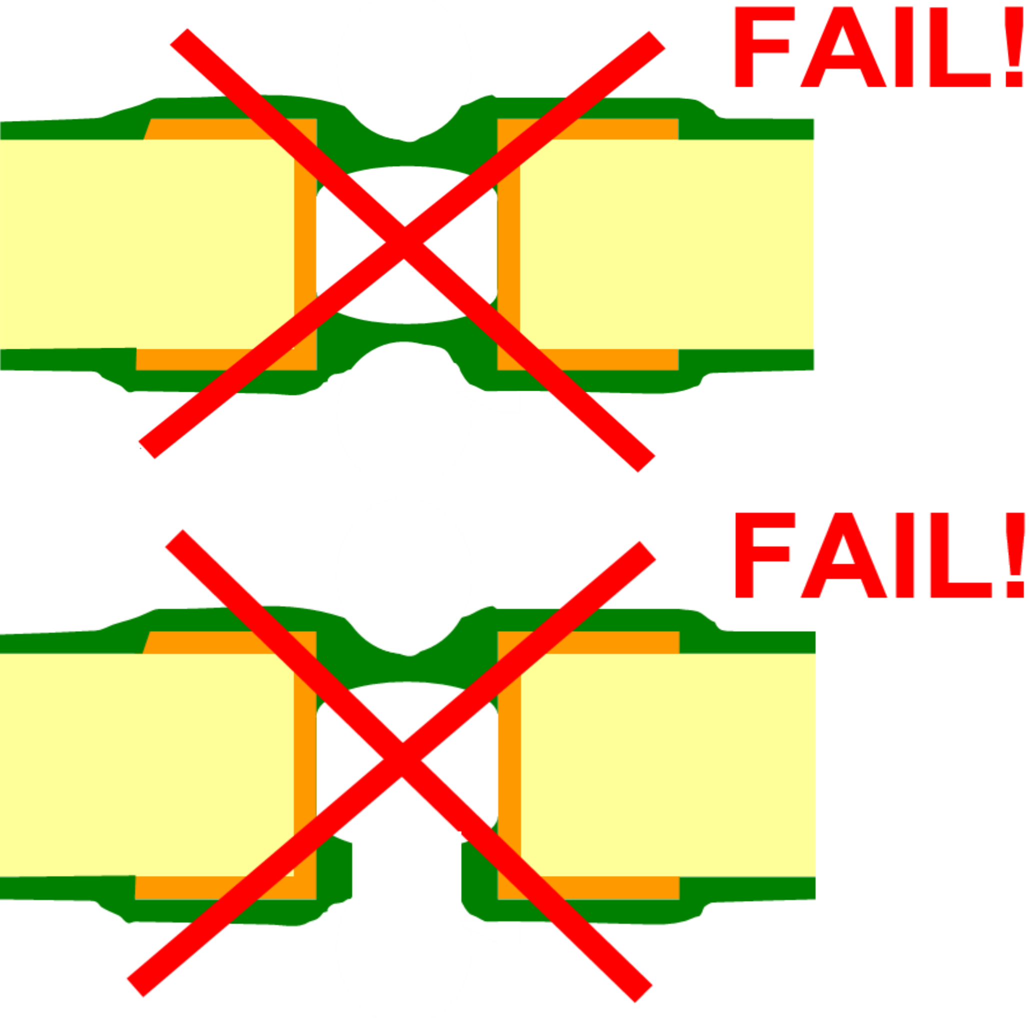
When **CASE 6** is required by MA file, via holes smaller than 0,5 mm diameter must be closed and sealed by solder resist like in following picture:

= base material = copper = solder resist



- no copper exposed (all copper is protected by solder resist).
- HASL balls or other foreign matters trapped into holes are NOT allowed.
- solder resist perfectly cured inside via hole.
- dimension "x" greater than 25 % of total PCB thickness.
- **for via holes with diameter ≥ 0,5 mm, follow CASE 1 (TQR §6.4.1).**
- **holes "tenting" not allowed! (see following pictures).**

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).



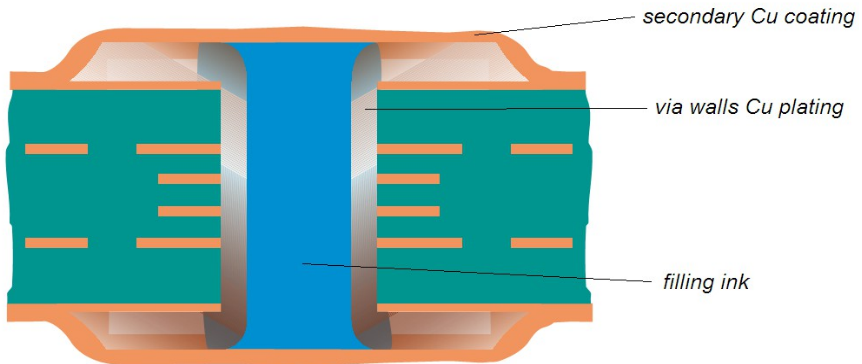
6.4.7. Via fill and cap (CASE 7)

When **CASE 7** is required by MA file, selected vias shall be completely filled-in and sealed with appropriate filling ink, then capped with a secondary metalized galvanic Copper coating covering the via on both sides, as showed in picture below.

If not otherwise specified in MA file, homologated via-fill materials are:

- ➔ Goal Searchers Zhuhai, GSH-00400.
- ➔ Taiyo, THP-100DX1 VF(HV).

<u>Should supplier want to propose a different via-fill material, see instructions at §2.3.</u>



Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Vias treatment shall withstand with no issues to thermal stress as per IPC-TM-650 2.6.8 (condition A); after test ink voids/cracks/recessions are not acceptable if exceeding 80 µm size or overall exceeding 40 % of via ink-height.

6.5. Peelable solder mask

When peelable solder mask is required in relevant documents, it must be applied as follows:

Peelable thickness on finished PCB: min 0,3 mm; max 0,7 mm.

Peelable solder mask must completely encapsulate the required area of coverage, and when applied over holes shall not protrude on the other side of the PCBs.

Peelable solder mask must be chemically compatible with all Selcom assembly processes.

If not otherwise specified on MA file, peelable solder mask must withstand with 3 consecutive lead-free reflow or wave soldering cycles, **and then must be easily removable with no residues left on the board surface or holes**.

Preferred models:

- ➔ PETERS, model “SD2954” or “SD2955”.
- ➔ Other models of “SD2950” series can be used depending on the particular application, supplier shall check it formerly with Selcom.

Any new peelable mask type could be used only after getting written approval from Selcom (see TQR §2.3).

Do not apply peelable mask on holes with diameter larger than 3,5 mm (see also TQR §2.16).

6.6. Silkscreen (Legend)

Silkscreen process (Legend) shall use permanent solvent-resistant ink, and patterns applied shall be in accordance with silkscreen gerber files.

If not otherwise specified in MA file, legend ink color shall be white over green solder mask (or over other dark-color solder mask); and black over white solder mask.

Any silkscreen marking over copper pads, conductors or any other copper patterns (even if covered by solder mask) shall be slightly moved away from those areas; if the moving is not possible, the marking shall be resized/reshaped to avoid the forbidden areas, unless it becomes unreadable or misunderstandable: only in this last case the involved marking shall be completely removed.

Legend areas different than alphanumeric symbols must be geometrically properly shaped and homogeneously filled as required in gerber files.

Anyway, if original gerber needs to be modified, please send it to Selcom for written approval.

Z-axis thickness of applied legend shall be the minimum possible, given the process is reliable and all marking are clearly readable. Total thickness from finished smd pads outer surface to the highest point on PCB shall be not greater than 95 µm.

Any case, no misunderstandable legend markings shall be visible on the board.

Any doubt, ask Selcom.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

7. TESTS

7.1. Visual test

The visual test is required for all the panels to exclude the presence of aesthetic defects.

7.2. Electrical test

100% electrical test has to be run on all the panels, and must ensure the following checks for all the conductors:

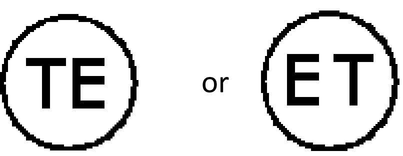
- ➔ absence of short circuits among conductor elements that are not connected
- ➔ electrical continuity of connected conductor elements.

The test shall be performed accordingly to IPC-9252A – Amendment 1 dated Oct 2012 (or latest revision issued), table 4-1, test level “C”, with rated voltage 250 V (or the highest voltage allowed by IPC-2221, table 6-1).

The PCB supplier is responsible for checking the efficacy and the range of the test.

Electrical test performed by PCB supplier shall be based on comparison with Selcom ODB++/netlist file or on an internal netlist with same meaning, 100% checked as matching with Selcom one (see §2.18).

The below marking must be inserted **after passing electrical test** on each single PCB present in delivery panel:



Any other kind/shape of marking for e-test must be preliminary agreed with Selcom.

Marks shall be made with a permanent ink able to resist to PCB and PCBA cleaning systems chemicals.

7.3. Mechanical test

Drilling, punching, v-cut and milling processes must be checked frequently to ensure that supplier production process remains within required mechanical tolerances.

In order to achieve this, a number of statistical process checks must be run (e.g. X-R check sheets) to prevent any defect to occur due to process drifts.

Punching tool wear must be kept under control by means of checking PCB edges roughness, amount of powder released, and mechanical measurements.

Punching tool must be sharpened regularly.

7.4. Scrap pieces

If not otherwise specified in MA file, no defective pieces are allowed in the batch.

(Refer. To §2.12, §2.13, §2.14).

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

Even when X-out (see §1.1) pieces are explicitly allowed by MA file, reliability defects (example: defects of galvanic copper plating; etc.) are anyway not tolerated and shall lead to the scrap of the whole delivery panel even if allegedly affecting just one piece in it.

7.5. Repairs and reworks

If not otherwise stated in MA file, some limited repairs/reworks are allowed. See also TQR §2.14. In any case all repairs shall meet the requirements of IPC-7711/7721, and repaired pieces must comply with all our applicable specifications.

Repairs on outer layer tracks or pads in BGA areas are anywhere not acceptable.

Repairs on outer layer tracks are anywhere not acceptable for IPC class 3 PCBs.

Repairs on tracks with controlled impedance are anywhere not acceptable.

The repair of open circuit shall be performed in accordance with procedure no. 4.2.3 of the IPC-7721. Repairs are allowed when interruptions or semi-interruptions occur on a track of an inner layer.

For outer layer open repair are **not** acceptable.

For the inner layers the repair is accepted only before the lamination.

Only opens on straight tracks far not less than 2 mm from hole pads are repairable.

The interruption gap to be repaired must not exceed the track width, and the cross sectional area of the weld material must not be less than the track under repair.

The weld material must have a visual appearance smooth and accurate.

Limits for interruption repairs:

Max. width of repairable conductors	*0,5 mm*
Max. interruption length	*3,0 mm*
Min. interruption distance from bump contacts or corners	*5,0 mm*
Max. number of repairs per track	*1*
Max. number of repairs for each panel	*2*
Max. number of boards repaired per supply batch	*3,00 %*

Conductor shorts repairs may be performed up to a maximum of 6 for any PCB, being sure that all aspects of our specifications are maintained after the repair.

For outer layers, a maximum of three shorts may be removed per PCB. Solder mask must be used to cover all such repair.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

The total thickness of repair plus covering shall not exceed 40 µm over the good tracks plane.

For inner layers, a maximum of three surface conductor shorts may be removed per inner layer. This operation shall be conducted before oxide treatment and lamination.

Mechanical repairs or re-welding of the plated holes are **not** allowed.
Repairs of lifted conductors and mounting pads are **not** allowed.

Solder resist may be restored in one point only of the delivery panel and along a maximum surface of 1 square centimeter, paying attention to not alter the aesthetic aspect of the board. Touch up ink shall be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder resist ink.

Repairs on the BGA areas are **not** acceptable.

The hole rework is allowed only for non-plated holes, to increase the diameter. This rework shall be done using only an automatic drilling/routing machine, avoiding any haloing effect on the holes edge.

The mechanical edge profile rework is allowed only to reduce the dimensions of the PCB to correct dimensions. This rework shall be done using only an automatic routing machine.

Reworks on surface finishings are acceptable only for HAL and OSP (with no change of alloy/model); only one rework is acceptable, with final quality results in compliance with Selcom specifications, and anyway not affecting in any way the solderability of the boards (see TQR §6.2).

For all other types of surface finishings, reworks are forbidden.

All boards must be 100 % electrically tested after repair/rework (see TQR §7.2).

Repaired and/or reworked boards must be packaged separately (see TQR §8.3).

All other kind of repairs/reworks not mentioned in Selcom specifications are to be meant as **not allowed**, unless prior written specific agreement of Selcom.

7.6. Microsection

In order to check actual build-up, per each new batch the supplier shall send to Selcom a physical microsection of the PCB, together with the original complete delivery-panel (free-of-charge) where the sectioned sample was cut from. The original date-code of the batch shall be visible on that panel as well as the position were the microsection was cut from.
In case of multilayer PCB, the microsection shall mandatory show ALL copper layers of PCB, and at least one of the internal layers connected to the via hole walls.
In case of PCB with blind and/or buried holes, the microsection shall mandatory show at least one buried and one blind hole for each kind of them (kind = technology used and connected layers). In case the layout makes not possible to group all above evidences in the same single microsection, more microsections shall be provided.

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

If physically possible basing on the PCB layout, in the same microsection it should be present at least also one PTH hole.
The sectioned via holes shall be chosen among the potential “worst case” ones of that board (example of worst case for galvanic Cu coating: from area with highest density of vias).
In case of complex PCBs, Selcom is available to evaluate a microsection performed by supplier on a custom test coupon built with the same batch into working panel breakaway, given the supplier shall preliminarily demonstrate to Selcom that the coupon performance is equivalent to the worst-case performance on the actual board.
The microsections shall be properly inspected by supplier before shipping the batch out; related photos and measurements shall be reported on quality papers attached to the batch (see §8.4, 8.5).
Microsection containing multiple holes is suggested. When inspecting a microsection with identical multiple holes, supplier shall visually inspect all sectioned holes, and measure the worst one.
In case the new date-code batch is shipped through multiple ways (e.g.: a part shipped by sea, another part by air, etc) the quality reports and the physical microsections shall be attached to the fastest shipment, so that they are got by Selcom together with the first received pieces.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

8. SUPPLY METHODOLOGY

8.1. Identification of the circuits

If not otherwise stated in MA file, the following items must be written onto PCB surface by supplier:

- ➔ supplier identification symbol (assigned by Selcom).
- ➔ batch code. This code must have the characteristics required by MA file. If any info about batch code is missing in MA file, then insert on PCB (solder mask) the week and the year of production.
- ➔ UL marks, if required in MA file.

All written codes must be placed by supplier in positions well visible even after Selcom will have soldered electronic components onto the PCB.

Any doubt, ask Selcom for a confirmation about each code position.

8.2. Cleaning operations

PCBs must be cleaned conforming to Standard

IPC-6012, latest revision. Right before packaging, the contamination level on bare PCB shall be not greater than an equivalent of 0,8 $\mu g/cm^2$ of Sodium chloride, measured in accordance with IPC-TM-650, Method 2.3.25, paragraph 4, Resistance of Solvent Extract Method.

PCBs must be devoid of witness marks, burrs of any kind, dust or encrustation; they must not have any signs of corrosion, fingerprints, labels or traces of any other foreign matters.

All circuits must be perfectly dried after washing, so to remove any excess of humidity. See also TQR §3.1 and §8.3.

8.3. Packaging

If not otherwise specified, all supplier packaging actions performed and materials used must be compliant with IPC-1601 standard.

Supplier must keep under control moisture level content in PCBs right before packaging: Maximum-Acceptable-Moisture-Content (or "MAMC", measured as per IPC-TM-650, Method 2.6.28) of PCB measured just before sealing its packaging bag must be not greater than 0,1 % of moisture weight to weight of resin and paper.

8.3.1. Moisture Barrier Bags

Primary packaging for PCBs must be heat-sealed Moisture-Barrier-Bags (or "MBB", as defined in IPC1601 standard), in order to avoid any contamination and preserve their dryness and perfect solderability until the expiration date.

All PCB panels in each MBB must be of same part number, packed with the same upper side and all facing the same direction.

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

All MBBs shall contain the same number of panels (except MBB with last remnant panels), and no more than 25 panels; given the gross weight of each MBB shall be no more than 5 kg.

Do not pack PCBs if they are warmer than +5°C over local packaging room temperature!

Some air evacuation from each MBB is necessary to prevent panels from moving/slipping during transportation. Anyway, in order to avoid applying excessive mechanical stress on panels, do NOT perform high-vacuum into MBB! Air suction shall reduce air pressure from min 75 % to max 85 % against environment pressure, that means final air pressure left inside sealed MBB shall be from min 15 kPa to max 25 kPa.

Panels shall not stick one another once the bag is opened.

For PCB with chemical surface finishings or with carbon contacts (see §3.8.1) supplier shall put paper sheets between all panels, included first sheet over first panel and last sheet below bottom panel. Paper shall be sulfur-free; with pH neutral; without fibrous residues on the edges. For the other surface finishings (HASL; OSP, etc.) the usage of paper sheets must be preliminarily allowed by Selcom.

One desiccant bag shall be inserted into each MBB, and placed along the edges of PCBs. Desiccant materials/quantity must be sulfur-free and conforming to IPC1601 standard, in order to keep the relative humidity inside the MBB to max 10% at 25°C for at least one year if MBB is stored at max 40°C and max 90% relative humidity.

Each desiccant bag must be dry and not exposed to air for more than 20 minutes before being sealed into the MBB.

Conforming to EU regulation# 2009/251/EC, all traveling goods and packaging materials shipped to European Union must be free from chemical substance Dimethyl fumarate or “DMF” (defined as CAS# 624-49-7 or EC# 210-849-0). Supplier must send to Selcom (once) a third-party laboratory certificate stating the desiccant bags used are free from DMF.

All MBB packaging materials shall be free from emission of sulphide, chlorine derivative or any other substance that could affect the solderability of PCB. MBB packaging film shall have enough mechanical strength to withstand to transportation solicitations without compromising the sealing properties of MBB.

Supplier shall use only MBB packaging materials showing in their data-sheet the value of Water-Vapor-Transmission-Rate (or “WVTR” or “MVTR”), measured as per ASTM F-1249 at 40 °C, after flex testing as per condition “E” of ASTM F 392.

For single-sided or double sided rigid PCBs with only one single standard rigid laminate in their build-up (only C-stage, no prepregs, no pressings):

- Maximum admitted WVTR of MBB packaging film is 0,180 grams/100inch^2/24hours, or 2,790 grams/m^2/24h.

For all the other PCBs (examples: multi-layers; flex; rigid-flex, etc.):

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

- Maximum admitted WVTR of MBB packaging film is 0,002 grams/100inch^2/24hours or 0,031 grams/m^2/24h. Be aware that simple clear plastic films without metallic layers in their construction typically do not fit above mentioned requirement! Refer to IPC-1601 standard for further details.
- Put one Humidity-Indicator-Card (or "HIC", compliant with IPC/JEDEC J-STD-033 and REACH regulations) inside each MBB, placed along the edges of PCBs (on the opposite side of desiccant bag) with colored dots faced outwards . HIC must be able to detect at least the following relative humidity thresholds: 10%; 30%; 60%. HIC material shall be free from emission of sulphide, chlorine derivative, Cobalt or any other substance that could affect the solderability of PCB.

Packaging performed by supplier shall be able to guarantee shelf-life of at least 12 months for PCBs inside sealed MBBs, stored at less than 40 °C and less than 90 % external relative humidity (see IPC1601, §5.2); any shorter shelf-life shall be based on third-party documents and needs Selcom preliminary agreement.

The following minimum data must be printed on a visible label attached on top of each MBB:

- ➔ Selcom complete part/number (as written in Selcom Purchase Order).
- ➔ Selcom MA file complete name and revision index.
- ➔ Full date-code (complete of supplier identification symbol assigned by Selcom), as required in MA file. Do not mix different part numbers and/or different lot codes in the same MBB.
- ➔ Number of single GOOD pieces inside the MBB.
- ➔ Expiration date of PCBs (expected to be minimum 12 months after original production date).

As widely acknowledged by international standards of electronics, baking can degrade solderability of PCBs! Supplier for first shall strive to avoid baking on finished PCBs, by practicing effective handling, packaging, storage, and process controls (ref. IPC1601 §3.4.1). Selcom does NOT require nor encourage supplier to automatically perform any baking or other conditioning/reworking on finished PCBs. Selcom will not consider and not accept any request nor instruction from supplier to perform baking on a good batch if it's still sealed into original PCB bags and still within its agreed expiration date at the moment of its usage. Any damage due to supplier's misunderstanding about this matter will be charged to supplier.

8.3.2. Carton boxes

Each carton box shall contain no more than 20 MBBs (all facing the same direction), given the maximum gross weight specified in PGR-SEL document is fit.

The following minimum data must be printed on a visible label attached on front visible outer side of each **carton box,** regarding the pieces contained inside it:

- ➔ Selcom part/numbers (as written in Selcom Purchase Order).
- ➔ Selcom MA file complete name and revision index.
- ➔ Full date-codes, as required in MA file (= supplier identification symbol + lot-code + other possible indications).
- ➔ Total number of single GOOD pieces.
- ➔ Expiration date of PCBs (expected to be minimum 12 months).

 Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).

- ➔ Origin country of manufacture (“MADE IN …”).
- ➔ **2D bar-code is required**. See separate specification, file “BCR-SEL” in last revision issued, which shall be checked and downloaded from Selcom website at:

  http://www.selcomgroup.com/SuppliersTechnicalRequirements

Refer to “PGR-SEL” document for other packaging details; last revision issued shall be checked and downloaded from Selcom website at:

http://www.selcomgroup.com/SuppliersTechnicalRequirements

8.3.3. Pallets

Refer to “PGR-SEL” document for all details; last revision issued shall be checked and downloaded from Selcom website at:

http://www.selcomgroup.com/SuppliersTechnicalRequirements

8.4. Documents enclosed with each supply

All documents and modules issued by supplier shall always include a proper translation in English language if they are addressed to a Selcom plant located in a Country speaking a different native language than supplier's one.

The following documents/materials must be issued by PCB supplier per each p/n and enclosed with each supply:

- ➔ Certificate of Compliance (=”CoC”, see §1.1), that shall include:
  - Selcom complete part/number (as written in Selcom Purchase Order).
  - Selcom MA-file complete name with revision index.
  - Formal declaration that the p/n has been produced conforming to Selcom requirements.
  - Type of PCB surface finishing (for HASL finishing just use the names “HASL leaded” or “HASL lead-free”, no other names).

    Note: in order to prevent misunderstanding, CoC of p/ns non-RoHS-compliant (example: PCB finished with HASL leaded) shall never include the word “RoHS”.
- ➔ List of raw materials (listed in §2.3) used for circuit production (brand and exact model).
- ➔ Measurements of the mechanical dimensions indicated as 'critical' or 'important' in MA file.
- ➔ Measurements of required controlled impedances (specify measurement method details).
- ➔ Measurements of thickness of each layer of the surface finishing.
- ➔ Measurements results of carbon pads resistance test; see TQR §3.8.
- ➔ Results of adhesion tests (see §3.8.4; §5.1 §6.1; §6.3).
- ➔ Above mentioned measurements/tests shall be performed on at least 9 delivery panels **randomly picked up** per each date-code, on at least 10% of single pieces (rounded to closer integer number) per panel (each piece taken the most distant possible from the others measured in the same panel), the same 3 finished pads per piece.
- ➔ Physical microsection of PCB (see §7.6) with related pictures and measurements.
- ➔ Electrical test Report, with indication of used voltage, percentage of coverage, and final result.
- ➔ Soldering test with description of the method, and physically attaching the tested board/sample.

- ➔ List of all date-codes/quantities inside each shipment (write it in packing list or in other relevant physical shipping document, and send a soft copy of it by email to Selcom).

Above mentioned documents and evidences shall be put into one single box clearly identified with external obvious signs and a label claiming "QUALITY DOCUMENTS INSIDE".

8.5. Documents enclosed with first supply

In addition to what required in TQR §8.4, these documents must be enclosed with first supply for homologation purposes:

- ➔ RoHS compliance declaration (only for RoHS compliant p/ns).
- ➔ REACH compliance declaration, to be re-issued again every time the related candidate-list-of-substances is updated on official website: http://echa.europa.eu/candidate-list-table
- ➔ Data-sheets of all raw materials used (see TQR §2.3).
- ➔ Other documents possibly required in MA file.

8.6. Documents format

All documents mentioned in §8.4 and §8.5 are required in a soft-copy read-only format (.pdf) sent by email (ask Selcom which email addresses to use, depending on the destination plant). A scanned soft-copy of original papers is acceptable if clear and well readable (min resolution 300 dpi, in colors where necessary). In order to prevent compatibility issues, file-names shall not include non-latin characters (e.g. Chinese chars).

Do not send single emails with total final size larger than 10 MB.

The only items necessarily required also in a hard-copy and physically attached to their related shipped goods are:

- ➔ CoC formal paper, showing all batch identification data and original signatures and stamps;
- ➔ microsections and other physical samples possibly required (test tapes, coupons, etc.).

* * * * * * * * * *

END OF TQR DOCUMENT

Selcom Elettronica S.p.A. is the owner of present document. All rights reserved (see cover page).